UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/826,067	04/04/2001	Matthew James Fischer	42146/RJP/E264	3885

23363 7590 08/16/2004

CHRISTIE, PARKER & HALE, LLP
PO BOX 7068
PASADENA, CA 91109-7068

EXAMINER	
LAM, DANIEL K	

ART UNIT	PAPER NUMBER
2667	

DATE MAILED: 08/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/826,067	FISCHER ET AL.	
	Examiner	Art Unit	
	Daniel K Lam	2667	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 April 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 April 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5/7/2002*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the features cited in **claims 4** (sending, receiving, and comparing timestamps, and adjusting slave clock) **and claim 5** (continue series of calculated master clock offsets and tracking error) must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

   Corrected drawing sheets are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. **Claims 1-5** are rejected under 35 U.S.C. 103(a) as being unpatentable over U. S. Pat. No. 6,665,316 issued to Eidson in view of U. S. Pat. No. 5,566,180 issued to Eidson et al (hereinafter Eidson180).

Regarding **claim 1**, Eidson discloses a time synchronization method in a distributed system 10 for controlling data sampling clocking of asynchronous network nodes (see fig. 1, nodes 20, 22, and 24, and col. 2, lines 16-22), each asynchronous network node having a local clock (local clocks 30, 32, and 34) and transmitting and receiving packets to and from an asynchronous network according to an asynchronous network media access protocol (the communication link 12 may be an Ethernet, token ring, or TDM; see col. 3, lines 1-9), comprising;

- Designating as a master node an asynchronous network node capable of transmitting and receiving packets on the asynchronous network (one of the nodes 20, 22, or 24 is a designated master node; see fig. 1, and col. 2, lines 30-32).
- Designating as a slave node each non-master asynchronous network node which desires to synchronously transport packets across the asynchronous

network (after designating a master node, the remaining nodes are designated as slave nodes; see col. 2, lines 32-35).

- Synchronizing a master node clock of the master node with a slave node clock of each slave node (the master node sends timing data packet and follow up packet to each slave node to achieve synchronization; see col. 2, lines 35-42).
- Deriving a derivative clock at the slave node from the continuously correcting each slave node clock to control data sampling at the slave node (any one of the nodes, 20-24, may be a sensor node which commonly contains analog to digital converter that requires the node to provide a clock for sampling analog sensor signal; see col. 2, lines 60-54.)

However, Eidson does not explicitly disclose:

- Continuously correcting each slave node clock compared with the master node clock to smooth slave clock error to an average of zero compared with the master clock as a reference using timestamp information from the master node.

However, Eidson180 discloses, by periodically comparing the node A (master node) clock with the node B (slave node) clock and adjusting the rate of node B clock, the clocks of the nodes will be in agreement. See fig. 11, and col. 8, lines 7-10.

Therefore, it would have been obvious to those having ordinary skill in the art, at the time of invention, to design a method of controlling data sampling having a designated master node as asynchronous network node capable of transmitting and receiving packets, a designated slave node, synchronize the master node clock

with the slave node clock, continuously update each slave node clock compared with the master node clock, and derive a derivative clock at each slave node to control data sampling, for a key reason. By having the clocks in the slave nodes synchronized with the clock in the master node, it allows successful operation of many measurement and control application the require precise timing control of events at several distributed locations (nodes) in the system as taught by Eidson180. See col. 1, lines 17-26.

Regarding **claim 2**, in addition to disclose the limitations in claim 1 discussed earlier, Eidson further discloses the step of designating a master node is determined by assessing an ability of an asynchronous node to directly access synchronous network timing information (Each node, 20-24, is directly connected to its local clock, 30-34. Each node also has a local clock information database, 40-44, containing information regarding whether the clock is a standardized timing source, whether the clock can be traced, an estimate of accuracy and jitter, etc. The local node compares the local clock information to the master clock information contained in the timing data packet to access the abilities of the clocks. See fig. 1, and col. 3, lines 34-65.)

Regarding **claim 3**, in addition to disclose the limitations in claim 2 discussed earlier, Eidson further discloses an asynchronous network node with direct access to synchronous network timing information is designated the master node (Each node has direct access to its local clock source. If the master clock information 52 within the timing data packet 50, or local clock information 44, indicate the clock source is a standardized timing source (GPS or atomic) with a

predetermined know stratum level, it is selected as master. See fig. 1, and col. 4, lines 41-53).

Regarding **claim 4**, in addition to disclose the limitations in claim 1 discussed earlier, Eidson180 further discloses synchronizing includes (see fig. 11, and col. 7, line 40 to col. 8, line 8):

Sending timestamp report messages in pairs from the master node slave nodes at periodic intervals (node a sends timing packets a1 and s1 to node b; see fig. 11, and col. 7, line 49 and line 53) by:

- Sending first timestamp report message from the master node to the slave nodes (node a sends timing packet a1 to node b; see fig. 11, and col. 7, line 49);
- Recording master timestamp information at the master node at a defined time during transmission of the first timestamp report message of a pair corresponding to the transmission of the first timestamp report message of a pair (node a records sending the first timestamp report message at ta1; see col. 7, line 49); and
- Sending a second timestamp report message from the master node to the slave nodes which contains the master timestamp information (node a sends timing packets s1 to node b containing timing information ta1; see fig. 11, and col. 7, line 53-54); and

Receiving timestamp report messages pairs by the slave nodes from the master node by:

- Recording a slave timestamp at the slave nodes at a fixed time during reception of each timestamp report message to provide a recorded timestamp of the first timestamp report message at the slave nodes (the timing packet a1 is received and detected by node b at recorded time of tb1; see col. 7, line 50);
- Comparing the recorded timestamp of the first timestamp report message of each pair at the particular slave node with the master timestamp information from within the second timestamp report message of the same pair to determine a master clock offset from the slave clock of the slave nodes (after receiving the second timestamp report message s1, node b compares an apparent time difference b-a of 140 ns; see col. 7, lines 55-56); and
- Adjusting the slave clock of the slave nodes to be synchronized with the master clock based on the master clock offset (node b resets its local clock back by 200 ns; see col. 8, lines 3-4).

Regarding **claim 5**, in addition to disclose the limitations in claim 1 discussed earlier, Eidson and Eidson180 further disclose:

- Using a continuing series of calculated master clock offsets from the slave clock to calculate a correction factor the slave clock, the additional calculated master clock offsets being determined from additional received timestamp report message pairs following the synchronization step (By using the timestamp report messages and local clock information, the slave node computes a correction factor, such as 200 ns; see Eidson180, col. 8, lines 3-4. Furthermore, suitable averaging of a series of measurements between the

master node clock and slave node clock may be made to reduce the effect of jitter; see Eidson180, col. 8, lines 12-13); and

- Tracking error of the slave clock as compared with the master clock and modifying slave clock frequency to smooth the error and create a continuously corrected slave clock with an average error of zero as compared to the master clock (Since each of the nodes periodically generate timing data packets (see Eidson col. 2, lines 30-32), the timing correction protocol between the master and slave node will be repeated periodically as shown in fig. 11 of Eidson180 (at times ta1 and ta2), over time, the slave clock will be continuously corrected with an average error of zero, such as apparent error and drift, as compared to the master clock. See Eidson180, col. 3, lines 23-30).

4. **Claim 6** is rejected under 35 U.S.C. 103(a) as being unpatentable over U. S. Pat. No. 6,665,316 issued to Eidson in view of U. S. Pat. No. 5,566,180 issued to Eidson et al (hereinafter Eidson180) in further view of U. S. Pat. No. 5,416,808 issued to Witsaman et al (hereinafter Witsaman).

Regarding **claim 6**, although Eidson and Eidson180 disclose the limitations in claim 1 discussed earlier, they does not disclose the step of deriving a derivative clock includes selecting a pair of integers to be used to divide in serial stages a synchronized tracked slave clock to a lower frequency to control the data sampling clocking.

However, Witsaman discloses a local clock source 46 having a divider 90 and a 32-bit counter 52 for deriving a derivative lower frequency clock to the timing

bus 60. The divider 90 and the 32-bit counter 52 are connected in series. See fig. 3, col. 6, lines 34-37 and lines 51-52, and col. 8, lines 44-47.

Therefore, it would have been obvious to those having ordinary skill in the art, at the time of invention, to design a method of controlling data sampling having a designated master node as asynchronous network node capable of transmitting and receiving packets, a designated slave node, synchronize the master node clock with the slave node clock, continuously update each slave node clock compared with the master node clock, derive a derivative clock at each slave node to control data sampling, and deriving a derivative clock includes selecting a pair of integers to be used to divide in serial stages a synchronized tracked slave clock to a lower frequency to control the data sampling clocking, for a key reason.

By having the clocks in the slave nodes synchronized with the clock in the master node, it allows successful operation of many measurement and control application the require precise timing control of events at several distributed locations (nodes) in the system as taught by Eidson180. See col. 1, lines 17-26. Furthermore, by having a local time signal that is synchronized with the master clock and at a lower frequency, the local time signal can be used by the local applications, such as the station controller in a paging broadcasting system as taught by Witsaman. See col. 5, lines 51-54.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel K. Lam whose telephone

number is (703) 305-8605. The examiner can normally be reached on Monday-Friday from 8:30 AM to 4:30 PM.

If attempt to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chi Pham can be reached on (703) 305-4378. The fax phone number for this Group is (703) 872-9314.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-4700.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status Information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DKL
August 1, 2004

KWANG BIN YAO
PRIMARY EXAMINER